Designing a two-channel data acquisition front-end board for a particle physics cosmic ray muon detector

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Abstract

At Brookhaven National Laboratory our group mission is the construction of a cosmic ray muon detector array. Our goal is to construct and place standalone detectors across New York State schools and colleges for gathering information about subatomic particles showers over a vast area. Every detector consists of three main components: a polyvinyl toluene plastic scintillator plate, a photomultiplier tube, and a data acquisition board. My part of the project was to prototype and develop the data acquisition (DAQ) board. The DAQ front-end board is an embedded system which includes amplifiers, discriminators, analog signal shapers, peak detectors, logic gates and multivibrator integrated circuit chips. The circuit board ought to identify the time of arrival of the particle which caused an electric signal, the energy deposited in the detector, filter the noise and hold acquired data for a necessary period of time to communicate with the Arduino board. One possible approach to designing the board is to simulate the circuit in a specialized software, create a printable layout design, obtain a prototype board, test for errors and if the prototype works as expected, submit for automated printing. The major update that was made to the previous design includes a two-fold digital logic component. The new design increases the accuracy and reliability of the recorded data and will be used in a new detector apparatus. As a result of this work, I have added circuit's simulation software (LTspice) to my repertoire of knowledge.

Introduction

The data acquisition front-end board is a circuit board that processes an electrical signal created by the part of the particle detector, a photomultiplier tube (PMT), executes the computing function of the muon detector and sends information for further processing. The proposed technical objectives of this circuit board included computation of the energy deposited by the particle in the detector, the noise filtering of the electrical signal, capability to adjust the threshold for a tested signal and ability to hold the acquired data for a necessary time to communicate with the rest of the data acquisition board unit, Arduino board. All the requirements were met including the additional objective of capability to adjust the duration of the accepting mode of the digital logic unit.

Process

The overall design schematic for the data acquisition front-end board is presented in Figure(1). Each OPA691 operational amplifier at the beginning of the system receives signal (sent from designated photomultiplier tube) through the Input_Connector_1_ACX1956-ND and Input_Connector_2_ACX1956-ND connectors. This part of the data acquisition front-end board amplifies the input pulse using a non-inverting amplifier circuit with a fixed gain and sends it for further computations. After amplification, this signal is split into two branches, digital and analog. An analog branch starts with the Shaper (THS4271 voltage-feedback amplifier), which is a part of the Peak Detector circuit. The shaper subcircuit is used to stretch and invert the signal for the upcoming peak detector unit. The peak detector unit (THS4271 voltage-feedback amplifier) purpose is to measure the peak amplitude that occurs in a waveform and hold this value, using an RC circuit. The next circuit component after the peak detector is the buffer (LTC6268 current feedback amplifier). A buffer provides an electrical impedance transformation from one circuit to another. Because the only summed signal is the subject of interest the role of this buffer is preventing the signal from peak detector to be affected by currents that the following component, the adder, may produce. The adder subcircuit takes in the two signals from their respective buffers and sums their averages, generating one output signal. It has a gain of 1 and does not invert the output signal.

A digital signal branch of the circuit starts with the discriminator (LT1711 rail-to-rail comparator). This sub-circuit is used to set a lower limit on the amplitude of the signal, this is implemented to filter the noise of the photomultiplier tube and increase the reliability of the data. The discriminator unit creates a square wave of an adjustable width and sends it to a coincidence logic unit. The and gate is a simple digital logic unit that computes logical coincidence. The and gate unit, working in conjunction with two discriminator units performs the processing power of the circuit board. This subcircuit computes whether the data should or should not be saved and stored. Only if the output of the digital branch is positive, calculated results of the analog branch will be saved. If none or not all inputs to the and gate are positive, low output results (0V) and no data will be collected by the data acquisition board. The next stage in the circuit is two monostable multivibrators. These integrated circuit components fulfill an objective of creating a time delay between digital and analog branches of the electric circuit. For the data acquisition board to operate correctly a digital signal of the circuit must be delayed due to the fact that an analog branch of the circuit requires approximately 80ns for computations. The first monostable multivibrator delays the incoming digital signal by 155ns and the second monostable multivibrator dictates the moment when the sample and hold unit must start sampling the signal

from the adder and provides 250ns to do so. The 155ns time delay is designated to provide enough time for the analog signal to stabilize at the adder output node. In the end, recorded adder output value will be stored on the sample and hold unit until the Arduino board reads it and sends a discharging signal back to the data acquisition board.

Discharge mechanism.

Once the Arduino (Arduino mega 2560) board records the analog value on the sample and hold chip, it generates a pulse of 6us and 5V and sends it to the discharge mechanism (BSS138). The short pulse activates the MOSFET (metal-oxide-semiconductor-field-effect transistor) transistor, allowing the peak detector subcircuit to discharge and therefore making the whole system ready for the next signal.

Progress

A design and simulation stages were completed utilizing the LTspice XVII, a freeware computer software implementing a SPICE simulator of electronic circuits, produced by semiconductor manufacturer Linear Technology. Altium, PC-based electronics design software for engineers will be used to create Gerber files (PCB fabrication data files), which later will be sent to a manufacturer for printing.

Conclusions

Simulating the circuit board, I used models of the real-world circuit components available on the market. Although the work was theoretical, a big progress in designing the schematics of the board was accomplished. The next step towards the goal of completing the circuit is to transfer the circuit schematics to another software for layout and prototype printing.

Circuit results are below.

Appendix

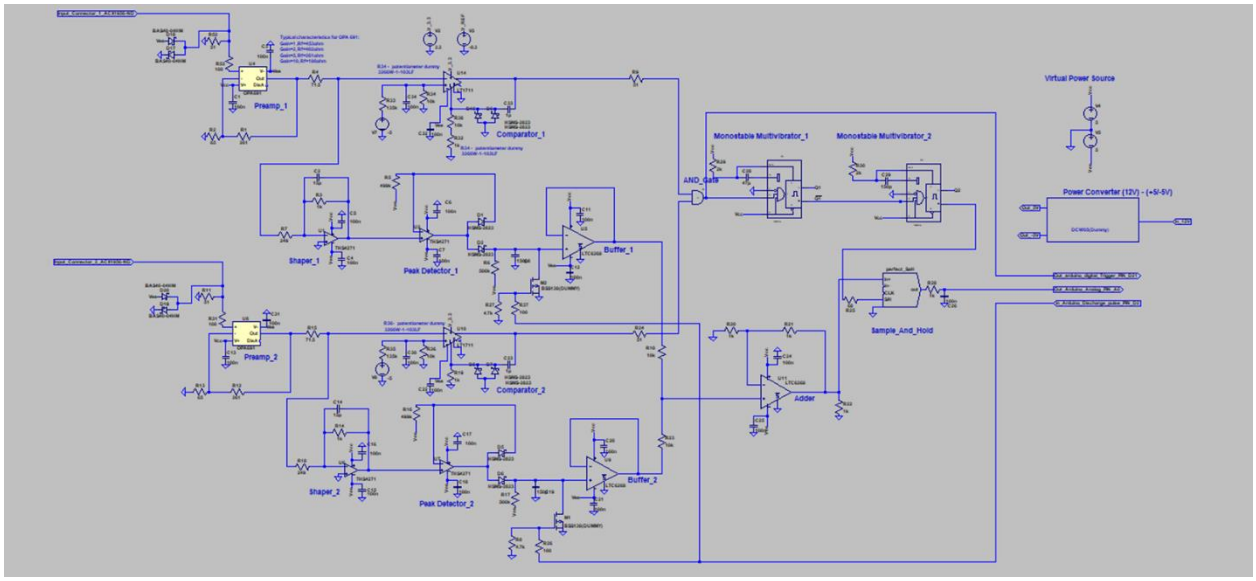

Figure 1. Overall schematic

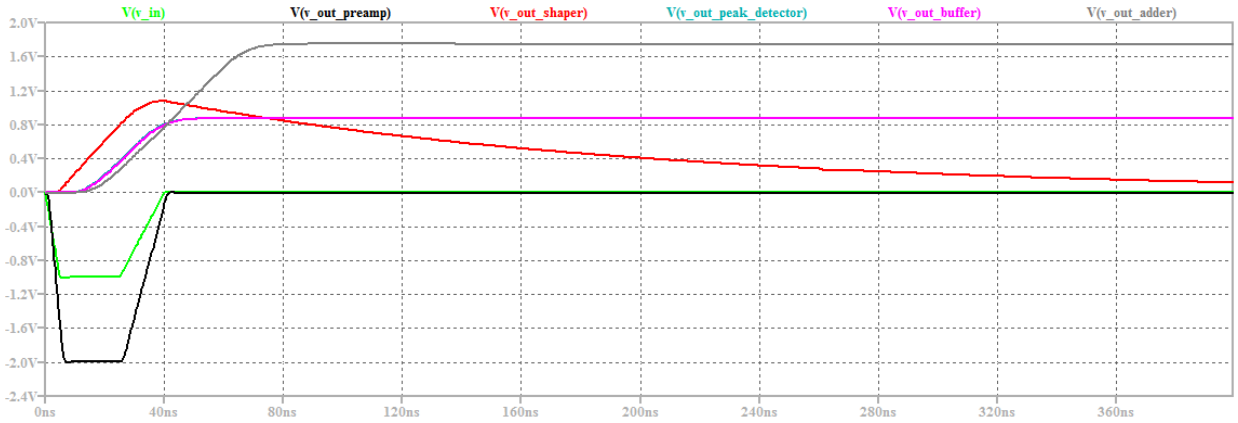

Figure 1. Analog branch simulation results

On the first set of waveforms we can observe the path of the analog signal to sample and hold unit. The waveform in green represents a generic PMT pulse going into the circuit. Next, pulse doubles its value due to the gain of two on the preamplifier (black waveform). After passing through the shaper the pulse is inverted and stretched (red waveform). The peak of the pulse is held after crossing the peak detector component (blue waveform, but it is overplayed by buffer). Buffer copies the peak detector pulse (pink waveform). In the end, when two pulses from different channels are added after adder component we can observe that the value got stabilized (grey waveform).

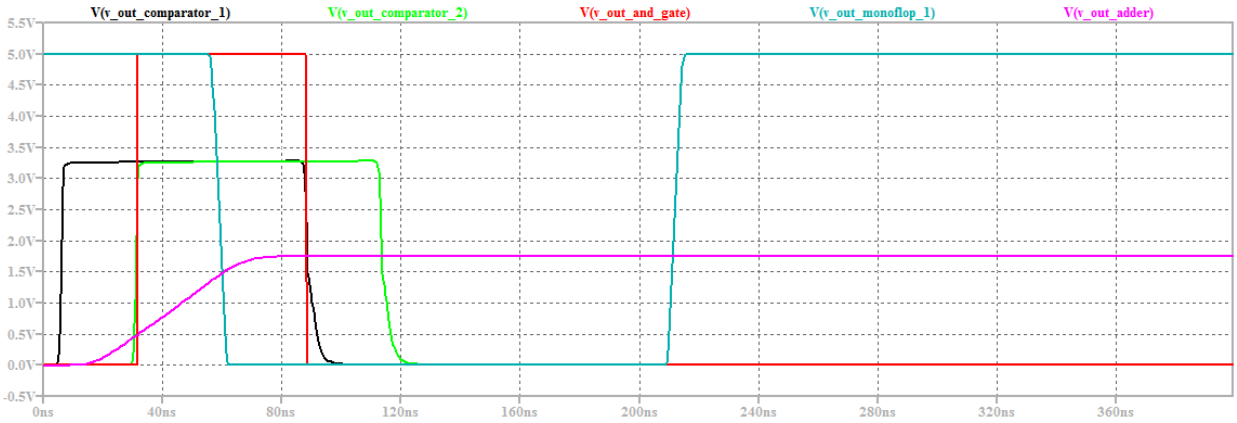

Figure 3. Digital branch simulation results

On this set of waveforms, we can observe the path of the digital signal to sample and hold unit. The waveforms in green and black represent comparators output signals. The next stage is AND gate. (red waveform). AND gate output is fed into monostable multivibrator_1, and we can see it's reaction signal in blue color. Due to computing power constrains I could not simulate the signal from the second multivibrator. However, you can observe that result on the right side of the poster. The final circuit component before sample and hold (SaH) unit, monostable multivibrator_2, will react to the first monostable and rise high for 250ns, giving enough time for SaH to detect stabilized voltage value of adder (pink waveform). Later this value will be sent to Arduino board and raspberry pie and saved in the data base.

Addendum.

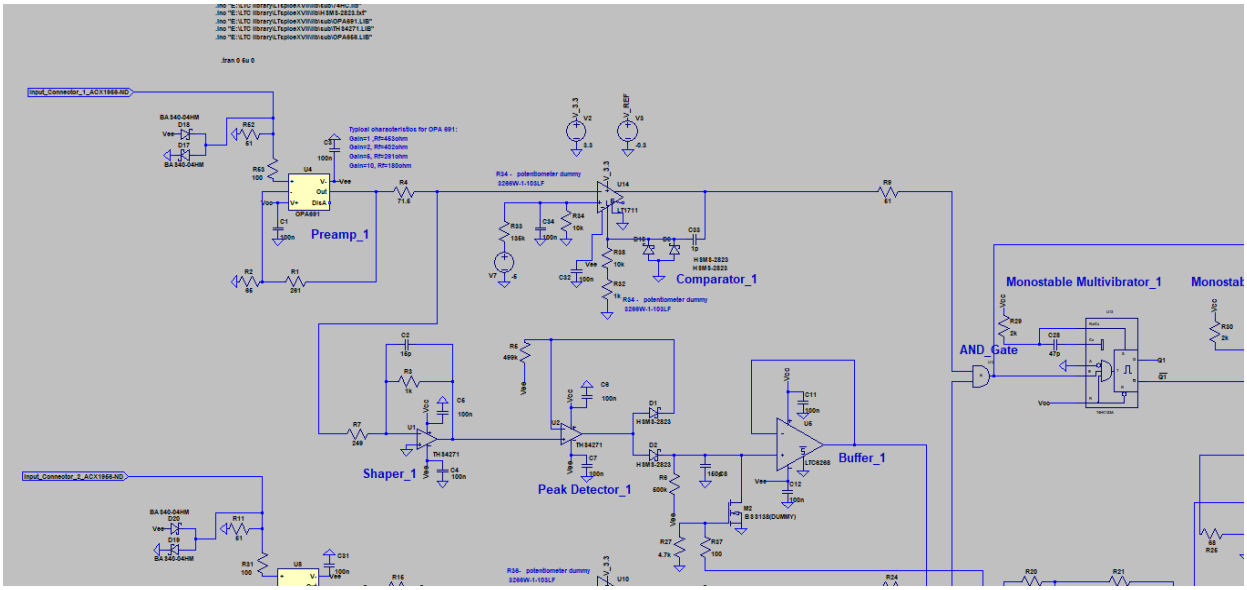

Figure 2. Upper-left corner of the circuit schematic

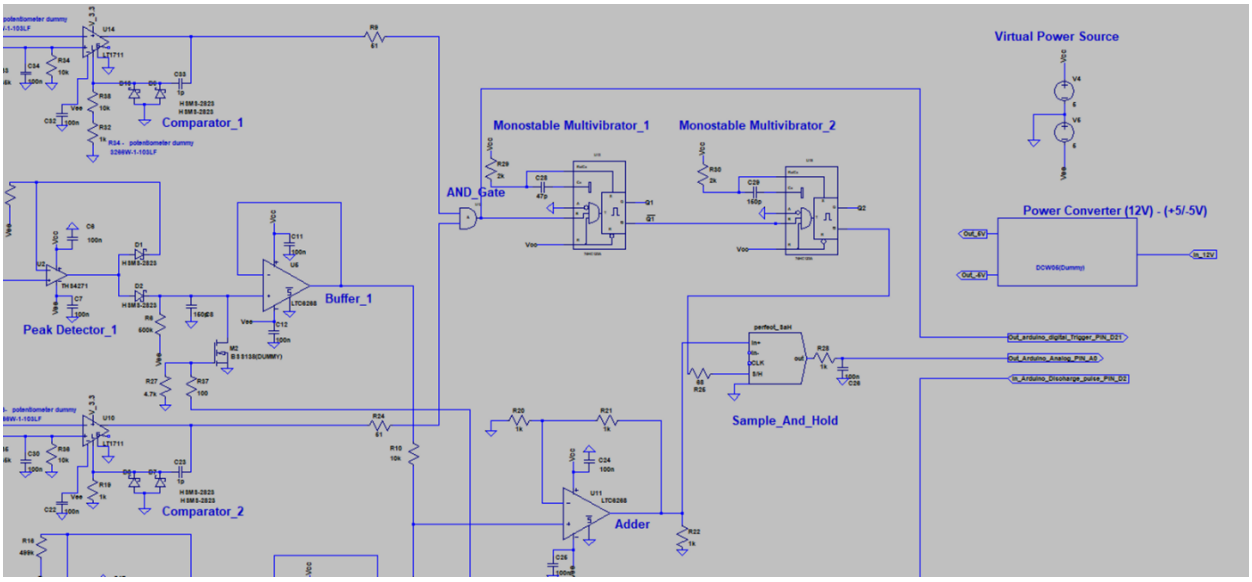

Figure 3. Upper-right corner of the circuit schematic

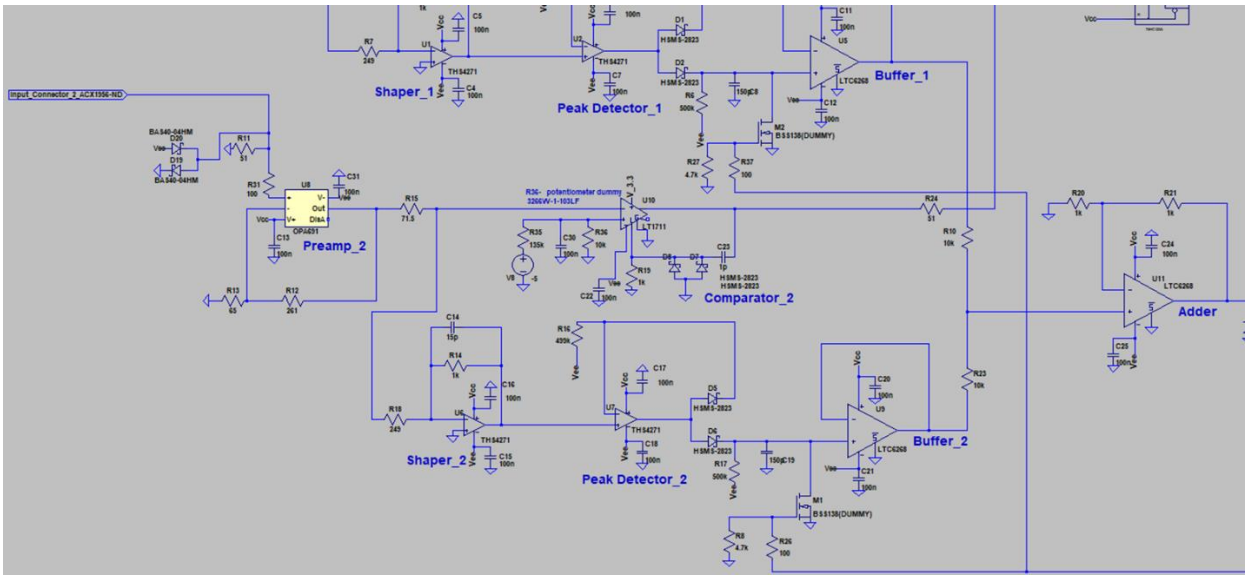

Figure 4. Bottom-left part of the circuit schematics

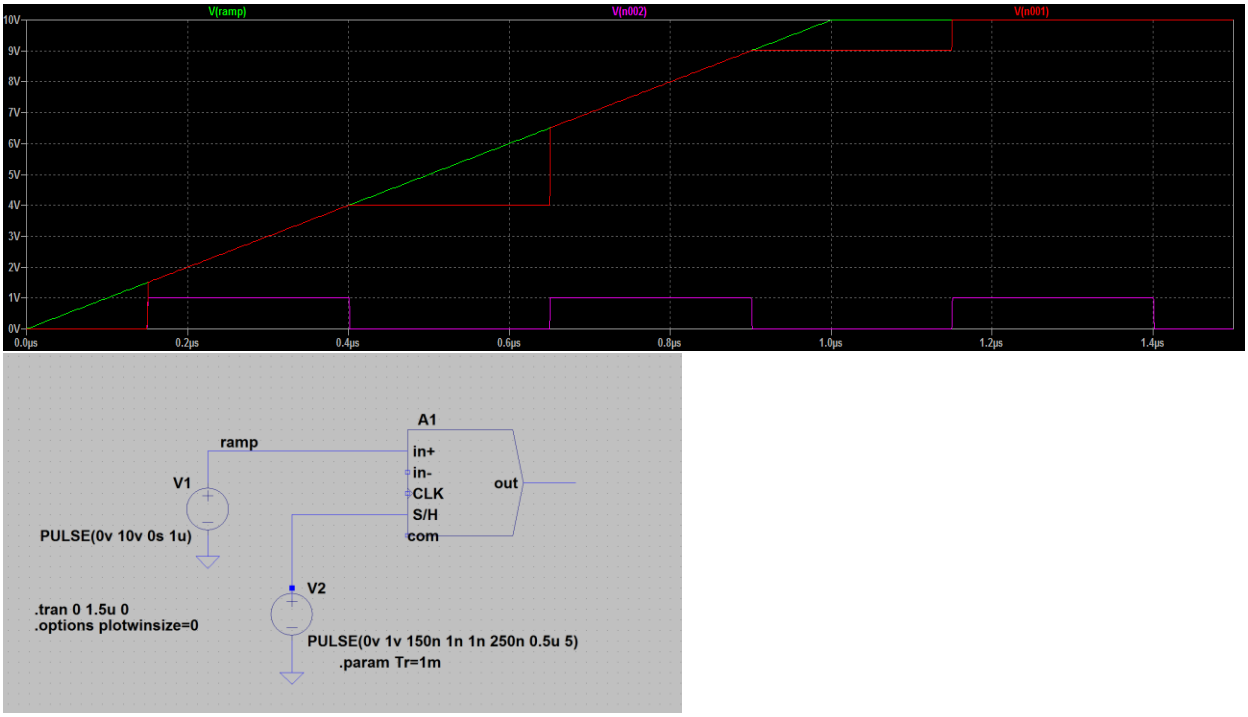

Figure 5. Perfect sample and hold simulation

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